

newsletter

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DECT ULP drives acceptance of wireless sensor networks

New ultra-low-power technology has momentum to become a Worldwide Technology Standard

A technology that has been commercially available for more than 15 years is gaining new momentum in the growing home automation, control and security network industry. Digital Enhanced Cordless Telephone (DECT) was once confined to commodity products such as consumer cordless phones.

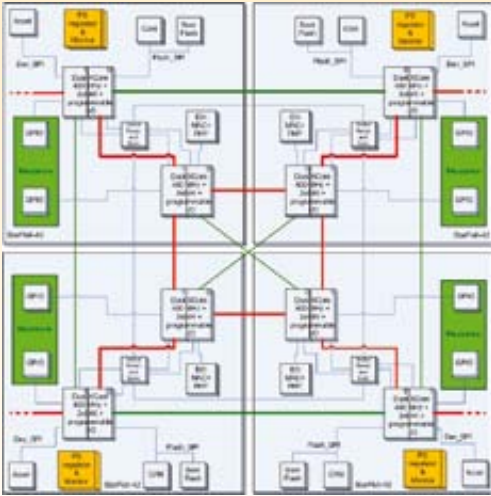


But with the recent development of the DECT ULP ultra-low-power operating mode, DECT is now opening up a new market for battery-powered wireless sensor / actuator networks.

continuation on page 3



Altreonic's StarFish scalable high reliability controller available for preview



Altreonic is now pre-announcing its new high reliability StarFish product range. Designed as a scalable and customizable range of embedded controllers, the StarFish architecture was designed to handle a wide range of real-time embedded applications. The basic building block is the StarFish-42. It has two dual-core 400 MHz 32Bit processors, each running up to 8 threads in the hardware.

Supported by the formally developed OpenComRTOS and supporting development tools, large networks of processing nodes can be transparently programmed. For this purpose StarFish hosts a wide range of communication and I/O capabilities like 100 Mbit/sec Ethernet, CAN and direct links for inter block communication.

This block architecture (without the mezzanine) delivers up to 800 Mips. The developer can exploit redundancy with synchronization and voting to increase the reliability of his design as an application option. More scalability and redundancy is provided by adding multiple StarFish-42 together as combined in the StarFish-424 where it delivers up to 6400 Mips. More of these modules can be linked together to create a distributed high performance embedded control system.

Application specific mezzanines allow the controllers to be adapted to a wide range of applications. Planned mezzanines will feature smart IO (Ethernet, CAN, SPI, I2C, PWM), programmable FPGA with analog I/O, DAC, ADC and high speed floating point DSPs.

Altreonic offers StarFish with a range of customization services: integration of C application code, programmable I/O, FPGA programming, custom mezzanine design and certification support. For the latter purpose, StarFish technology will also be made available under an Open Licensing scheme. First engineering systems are expected in 4Q of this year.

Interested customers who want more details or who want to consider application specific designs are invited to contact us at [info.request \(@\) Altreonic.com](mailto:info.request@Altreonic.com)

More information can be found in the preliminary product leaflet on [www. Altreonic.com](http://www.Altreonic.com). ■

Smart Energy versus Energy Saving: the search for ultra-low power technology?

Energy is recognized as one of the global grand challenges. The energy debate is mainly about renewable energy and about smart grids, the energy networks intelligently managing the alternative energy sources and a more flexible energy consumption, with attractive pricing for the consumers.

It remains however a very clear fact that the cheapest energy is the energy which is not consumed. Energy saving should be the most important aspect in the energy debate. Interesting energy saving technologies and application scenarios are already being developed: car manufacturers like BMW and Audi are installing electronic devices, temporarily stopping the car's engine while waiting at a traffic light. Research is being performed about saving energy in production machinery.

Also in the ICT-sector, a lot of power can be saved in electronics circuitry. Today, a lot of energy is wasted by consumer electronics and communication devices, by an "always on" utilization. However, is it necessary to have your modem switched on, while nobody is at home or while you are sleeping? And even when switched on, energy consumption can still be reduced.

Since many years, the DSP Valley members have world class competencies in chip design for ultra-low power applications. As a heritage of the research of Professor Hugo De Man, ultra-low power design methodologies have been developed in our region, now being used or being commercialized by spin-off companies and other adopters in the region. Ultra-low power chips and IP blocks, both for digital and analog technologies, have been designed and brought to market. This tradition in

ultra-low power design is fully alive and kicking: it is proven by the yearly papers and prototype chips being presented at ISSCC by DSP Valley members. And probably, most modern hearing devices, from wherever in the world, are using technology, chips or design tools, developed in the DSP Valley region around Leuven in Belgium and Eindhoven in the Netherlands.

Whenever you are looking for modern ICT for drastically reducing the power consumption in your application, don't hesitate to come and look for solutions in our region! Since many years, we have best in class technology, and we are fully prepared to keep this pole position in the coming years!

Sincerely
Peter Simkens
Managing Director
DSP Valley



continuation from page 1

DECT ULP drives acceptance of wireless sensor networks

New ultra-low-power technology has momentum to become a Worldwide Technology Standard

The development of DECT ULP was spearheaded by RTX Telecom A/S and SiTel Semiconductor, a Dutch company that spun out of National Semiconductor in 2005. Today, SiTel is a leader in low-cost silicon solutions for mid-range and high-end DECT applications and has a 35% share in the worldwide cordless telephone market. Its chips are also found in baby monitors, healthcare and enterprise systems, and controllers for the Xbox games console.

SiTel has always differentiated itself with low-power solutions. It has a long-standing commitment to provide more environmentally friendly solutions for powerhungry mobile devices. This drive for ecological innovation in telephony resulted in the company winning the 2009 Frost and Sullivan Global Enterprise VoIP Semiconductors Green Excellence Award in Product Innovation among many other industry accolades.

That drive also led to the creation of DECT ULP, making it possible for manufacturers to develop a whole new class of devices – DECT-based sensors and actuators. DECT ULP can manage and control everything from security to healthcare and comfort applications. Moreover, it enables 'fix-and-forget' sensor nodes that operate for over 5 years on a single AAA battery.

Generating buzz

DECT ULP was introduced to the world in February 2010 at the DECT World Congress in Amsterdam. SiTel, together with Danish firm RTX Telecom A/S and German companies AVM and Gigaset Communications, presented a live demonstration of a working sensor module.

That appearance certainly made a big impact. At the end of the Congress, attendees voted DECT ULP as the biggest expected future growth scenario for DECT and DECT-related technologies. The four companies have since formed a consortium and working group to investigate the requirements for getting the DECT ULP proposal approved by the European Telecommunications Standards Institute – a move that has gathered a lot of momentum.

"The technology and the live demo generated a huge amount of interest and positive feedback at the Congress. That shows there is a massive market opportunity for everyone involved in DECT and wireless sensor networks. We believe the window of opportunity is here, and the reaction from the DECT World audience tells us that the DECT industry is ready to take DECT ULP to the next level," said Jos van der Loop, Product Marketing Manager at SiTel.

The obvious choice

DECT ULP is an ultra-low-power operating mode of the familiar DECT protocol. Leveraging the reliability and consumer market experience of the large installed base of cordless telephones, it gives application developers the comfort of a proven standard and adds high voice quality as an attractive differentiating feature.

For consumers, DECT ULP promises easy network installation and expansion with push-button registration of new nodes. It operates in a licensed but royalty-free frequency band and allows a large number of nodes to function reliably at the same time.

"DECT ULP inherits all the range, installed base and cost benefits of DECT, and meets consumers' home sensor network needs without the interference issues, limitations and disadvantages of other proposed network protocols. We've clearly shown that it's the obvious choice for home automation, control and security systems," van der Loop concluded. ■





Six VUB excellence centers for strategic research – privileged partners for innovation and projects together with industry

The Vrije Universiteit Brussel (VUB) has chosen to concentrate its IOF funding (Industrial Research Fund) in a limited number of strategic research themes. An internal competition, based on the applicants' visions, roadmaps and performances concerning knowledge, innovation and technology transfer, led to the selection of 6 IOF-cores and 3 IOF-growers.



Biomedical research at ETRO, e.g. systems for medical and dental industry

IOF-cores:

- electronics and informatics (ETRO)
- applied physics and photonics (TONA)
- industrial microbiology and food biotechnology (IMDO)
- diabetes (DRC)
- chemical engineering (CHIS)
- surface and material engineering (SURF)

IOF-growers:

- robotics and applied mechanics (MECH)
- toxicology and dermato-cosmetology (FAFY)
- molecular and cellular therapy (LMCT)

As from now, a brand new brochure describing their core competences is available at http://www.vub.ac.be/downloads/IOF_fiches_2010.pdf. All of these groups are committed to accelerated and effective transfer of scientific results and technology to industry and society. Their goal is to maximize the following KPI's: **new spin-offs, portfolio of activated patents, collaborations with industry, government and non-profit sector, a leading role in their field in European R&D projects and programs.** The IOF groups exceed the average scale of a university's research unit. IOF-'cores' and IOF-'growers' are carrying out a substantial amount of strategic research that leads to application-oriented inventions with economic and societal value.

The Electronics and Informatics department (ETRO) is the IOF-core in ICT at

Previewing C vfAnalyst Parallelization Features with vFLabs



vfAnalyst is a cloud-based tool that helps software engineers parallelize C programs for embedded systems. You can look at hot spots, see complex data dependencies, prompt for partitioning options – with their benefits and costs – and then decide which to implement, iteratively improving the performance of your program.

This is a capability that vfAnalyst has only recently made possible; no other tool like it exists, so it's doing things that haven't been done before. Thus, while some features of the tool will be obvious, there are other ones that may not be so clear.

This is complex stuff, and there's often more than one way to solve a problem. Engineering and marketing can argue for hours about how a feature should work, but users can settle the discussion with much more authority.

To address this, Vector Fabrics has just released vFLabs, a means of trial-previewing new C parallelization features. As an example, with the latest release of vfAnalyst, Vector Fabrics released several key new features to production – including a speedup indicator (showing the cumulative speedup provided by all of created partitions) and data parallelism – but reserved three new features for further refinement by releasing them through vFLabs.

One of the new vFLabs features is a C library, called vfStream that imple-

ments streaming data communications between threads. vfAnalyst simplifies the collection of information you need to make partitioning decisions, but implementing those decisions from scratch is tedious and error-prone. The vfStream library eliminates much of that effort and risk; vFLabs will let you confirm whether it's complete and ready for prime time.

Two other vFLabs features affect the vfAnalyst display: one shows an ASAP execution schedule for parallelized loops, the other provides a skyline display of CPU usage. In both cases, your feedback determines whether these displays are easy to understand and use, or whether a different approach might be more effective.

When you enable a vFLabs feature, Vector Fabrics solicits feedback through a brief survey about the feature. While you can



Optrima's 3D camera

the Vrije Universiteit Brussel. It hosts 3 research groups: micro-electronics (LAMI), multidimensional signal processing and communication (IRIS), and digital speech and audio processing (DSSP). These three subunits deliver unique value through beyond-mainstream, multidisciplinary engineering research, such as:

1. Combined physical image generation and image processing for superior imaging systems (LAMI and IRIS) - 2D/3D imaging & 3D cameras; mm-wave & THz sensing
2. Audiovisual signal processing for man-machine communication (IRIS & DSSP) - Audiovisual interaction in multimodal communications; Audiovisual emotion and gesture analysis & synthesis; Source localization and tracking in audiovisual scenes

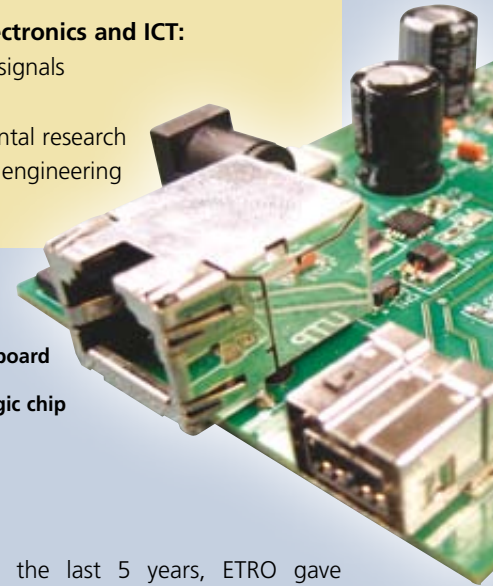
3. ICT Systems and applications based on wired/wireless communication on broadband networks and ad hoc sensor networks (IRIS) - Digital watermarking for quality testing and content filtering; 3D visualization and coding; Wireless communication and applications



The applications of Universum Digitalis run on a smartphone or a PDA.

ETRO- Crossing boundaries with visionary electronics and ICT:

Making sense of audio, video, hyper-dimensional signals & sensors for various sectors
 Beyond mainstream demand-driven and fundamental research
 Delivering unique value through multi-disciplinary engineering
<http://www.etro.vub.ac.be/>



Printed circuit board with Eqologic chip

During the last 5 years, ETRO gave birth to three spin-off companies: **EQCOLOGIC** (based on technology regarding communication equalizers, low-power and general-purpose integrated circuits), **UNIVERSUM DIGITALIS** (a service-based company specialized in the deployment of customized solutions for mobile media management and distribution) and **OPTRIMA** (leader in hardware for 3D gesture interfaces).



be as detailed as you want in open-ended comments, you can also quickly provide simple responses in a few seconds if you have little time. These answers are of enormous value in validating complex new capabilities; they will have a direct impact on your experience. Even though the vFLabs features aren't

fully released into the production tool, they are of production quality; this is not a way of slipping beta-quality features out early. You're not testing the quality of the code; you're just testing the way the feature works. Based on your input, the features may be released as is, they may be changed

before release, or they may not be released at all; one way or another, they migrate out of vFLabs – into the full tool or into the trash. Meanwhile, other new ideas take their place in vFLabs, keeping it going as a valuable forum for developing new capabilities to make your life easier.

About Vector Fabrics

Vector Fabrics simplifies the process of parallelizing C code for both enterprise and embedded applications, providing navigation aids for multi-threading and turning a months-long error-prone process into a manageable correct-by-construction task. Its first product, vfAnalyst, can assist in the parallelization of any C program on a system-agnostic basis. Vector Fabrics tools are hosted in "the cloud" and are accessible by any standard browser. Vector Fabrics is based in Eindhoven, the Netherlands.



Tools for building mathematically verified software

Verum and Solidsource close technology partnership agreement

ASD:ModelBuilder will deliver state-of-the-art user experience based on SolidSource technology

Verum Software Technologies B.V. (Waalre) and SolidSource (Eindhoven) have closed a technology partnership agreement that will see the two companies working closely together on the development of new software engineering technologies. Initially the partnership will focus on applying SolidSource's expertise in translating complex infor-

mation into simple, easy to understand graphics to enhancing the way that Verum's ASD:Suite displays information to and interacts with the Software Engineer.

SolidSource will study the typical work-flows and use cases of ASD:Suite users and will optimize the design, presentation and ergonomics of the

ASD:ModelBuilder to deliver a state-of-the-art user experience to Software Engineers. The goal will be to delight the end user and to increase their productivity beyond the groundbreaking level of 20 delivered ELOCS/man hour typically reached by most ASD customers today.

In the future Verum and SolidSource plan

AnSem offers a complete development package for SerDes



Over the past years, AnSem has accumulated a very broad experience in the development of SerDes (Serialiser-Deserialiser) IP for different standards like SONET, XAUI, PCI Express, Rapid I/O, ... These IP are available across a range of different foundries and technology nodes. This has resulted in a set of state-of-the-art silicon proven SerDes IP meeting all industry requirements in terms of area, power and speed.

Key features of AnSem's SerDes include multiple data rates up to 10Gbps, various I/O interfaces (LVPECL, LVDS, SSTL, ...), various clock-and-data recovery architectures (phase interpolator-based, PLL-based), jitter tolerance > 0.65UI and transmit jitter < 0.1UI.

As part of its design service activity, AnSem has offered for years the development of custom SerDes meeting the specific requirements of the customers in

their applications, and it will continue to do so. Moreover, customers sometimes need more than a custom SerDes IP, but want to develop their own SerDes roadmap for the future.

To address this need, AnSem has worked out a complete SerDes development package that allows customers to develop their own roadmap based on a set of silicon proven SerDes IP. This development package includes the design information and design documentation of SerDes circuits developed and qualified by AnSem. All this comes along with an extensive complimentary support package consisting of both on-site and remote support by AnSem's SerDes specialists.

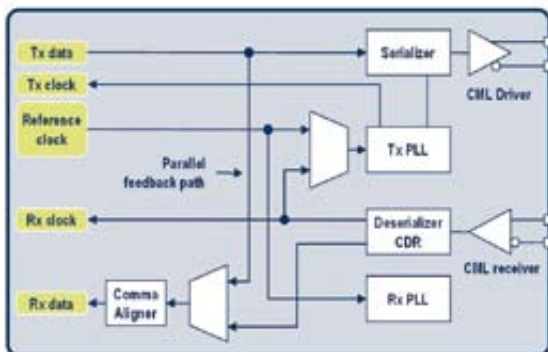
Moreover, the SerDes development package includes advanced design scripts containing in-depth design know-how of the critical parts of the SerDes. Examples of these scripts are a Matlab script to model the different sub-blocks of a PLL

and their interaction, as well as a generic VHDL model for phase interpolator based clock-and-data recovery architectures.

This SerDes development package targets customers who want to roll out their own SerDes roadmap and provides them a head start based on state-of-the-art knowledge accumulated over the last decade. The silicon proven IP and the extensive support provided by AnSem's SerDes specialists enable a fast and low risk development of their own SerDes roadmap. ■

About AnSem.

AnSem is a fabless IC design company, founded in 1998. Specializing in the state-of-the-art design of high-performance analog and mixed-signal integrated circuits in the most advanced technologies, AnSem offers design services and products for wireless communication, high-speed data communication and data acquisition. AnSem provides cost-effective turnkey solutions using the latest technology with emphasis on best time to market. The company is based in Leuven, Belgium, home to Europe's DSP Valley technology network organization, and is a member of the DSP Valley and the Global Semiconductor Association (GSA).



to integrate SolidSource's cutting edge software analysis products into Verum's SaaS hosting environment, allowing SolidSource to offer its products and services to a wider range of customers on a highly flexible, pay-as-you-benefit basis. Margaret Menzies, Director of Product Development at Verum said, "Our new partnership with SolidSource will not only help make ASD:Suite's unique technology more accessible to a broader range of technical users, it will also be a very appealing tool to use. We have already begun using SolidSource's expertise to make the ASD:Suite product more intuitive and visually efficient for all types of general software development."

About Verum Software Technologies B.V.

Verum Software Technologies provides a software engineering toolset that enables customers to rapidly develop defect free software for complex systems. Experience has shown that customers using the ASD:Suite can typically reduce the cost of developing their software up to 75% and in equal decrease in time to market, achieving ROI within 3 months. The application of the ASD:Suite also results in a large decrease of the cost-of-non-quality and thereby increased customer satisfaction. The difference between the ASD:Suite and other similar products is that at the heart of ASD's model driven tooling there is a patented formal verification engine that mathematically ensures the completeness and correctness of any software designed and generated using the ASD:Suite.

Lucian Voinea, CEO at SolidSource said, "We believe that the application of SolidSource's expertise in software visualization technology to Verum's ASD:Suite will lead a quantum leap in

the usability of ASD. Equally, we are extremely interested to see how we can use Verum's SaaS technology to bring our own product range to a wider audience." ■

Sigasi announces first round funding

High tech company financed by Belgian venture capital

Sigasi, a Ghent-based high tech EDA start-up, announced that it has closed its first round of funding. After two years of development, market validation, and a product launch, the start-up is ready for its next step.

Sigasi was founded in January of 2008 by two PhD's from Ghent University. The company was initially financed by seed capital provided by the founders, by subsidies from the Flemish Agency for Innovation through Science and Technology (IWT), and by a mezzanine loan from Flemish Innovation Fund (Vinnof).

After two years of development and a successful beta-testing program with several customers, Sigasi released its flagship product *Sigasi HDT* in January

2010. Sigasi HDT had a successful start, being sold worldwide, in many industries including consumer electronics, automotive, and aerospace.

Triggered by this success, Sigasi was able to attract additional funding. The investors in this round are: Baekeland Fund II, the venture seed fund of Ghent University; business angels; and the team.

Sigasi innovates in the domain of Electronic Design Automation (EDA) in two important ways. "First, it produces a novel intelligent development environment (IDE) for digital circuit design. The idea of this IDE is based on modern software development platforms, like *Visual Studio* and *Eclipse*," explains Philippe Faes, Sigasi co-founder and CEO. "Second, Sigasi is a native web-based company that employs an innovative

low-touch sales process. The whole process, including distribution, sales, communication and support, happens over the Internet. This is very different from the traditional direct sales methods in EDA."

"Now that we have this funding, we will be able to develop our products faster and provide better customer support. We are currently hiring additional engineer staff, to help bring our VHDL development environment to the next level" says Hendrik Eeckhaut, Sigasi co-founder and CTO. ■

Sigasi
automated hardware refactoring



Q-Star Test and BEST-IIC announce a strategic cooperation ...

...serving the Taiwanese market with solutions targeting product quality improvement and test cost and time-to-volume reduction, based on the application of Q-Star's unique supply current (IDD) test and measurement solutions combined with BEST-IIC's test program development services.

Q-Star Test, an innovative supplier of precision IC test and measurement instrumentation and a global leader in advanced high speed high accurate current test and measurement solutions, announces that Back End Service Trade Intelligence Integration Corp. (BEST-IIC), a Taiwanese semiconductor testing firm, has become a distributor of Q-Star Test products. The agreement extends sales and technology support for Q-Star's technology solutions throughout Taiwan.

Q-Star Test offers IDDX measurement instruments and related solutions, supporting a cost effective application of true IDDQ, Delta-IDDQ, advanced IDDQ, IDDT and analog IDD test strategies to digital, analog, and mixed signal circuits, thereby improving product quality and lowering down the cost of test. Q-Star Test's measurement hardware is ATE independent and outperforms other available ATE related IDD test hardware by at least a factor of 100 (with respect to measurement speed) and offers in addition a 10x improvement in test data quality (with

respect to measurement resolution and repeatability). The hardware solutions are complemented with application and test strategy related consulting and training services.

BEST-IIC, based in Kaohsiung City, Taiwan, specializes in integrated circuit test program development, automatic test platform conversion, and total test services from design-for-test to production, as well as software and hardware.

Justin Huang, BEST-IIC Sales Manager said, "Our 10 years' experience satisfying IDM firms, IC design houses and dedicated test firms allows us to focus on



The Current Test Company

our customers' test cost reduction, quality and yield improvement. We are very enthused about promoting and applying Q-Star's unique intelligent precision measurement instruments and test solutions."

According to Q-Star Test's CEO Hans Manhaeve: "We are pleased to team with BEST-IIC to offer more value to our customers, deploying our advanced high speed high accurate current test and measurement solutions, which are critical for ASIC design houses, test service suppliers and foundries in Taiwan. In addition as a result of our joint efforts TSMC has selected one of the Q-Star products for an application related evaluation" ■

About BEST-IIC

BEST-iic, based in Kaohsiung City, Taiwan, was founded in 2005, specializes in integrated circuit test program development, automatic test platform conversion, and total test services from design-for-test to production, as well as software and hardware. The firm represents test related products helping customers to improve test quality, reliability and efficiency from development to production. With over 10 years experience in IC testing and customer services, the firm provides the best solution out of customer's requirement.

DSP Valley visit to Japan



DSP Valley visited Japan from 10th till 14th May with a delegation of its members: Altreonic, AnSem, NXP Semiconductors and Target Compiler Technologies.

Not hampered by any volcano, the DSP Valley delegation arrived on time in Japan and held a first seminar on Monday 10th at the new Belgian Embassy in Tokyo.

With 47 participants the seminar was very well attended. After the opening speech given by the ambassador, several presentations have been given by the DSP Valley companies present. The reception after the seminar was hosted by FIT; the new Belgian Embassy really appeared to be an exquisite location for such an event.

On Tuesday 11th May the whole delegation travelled by Shinkansen to Osaka for a second edition of the seminar. The Shinkansen (also known as the bullet

train) is really impressive. With a departure frequency of every 10 Minutes (like a European metro) the Shinkansen 400m long and with over 1000 passengers on board (twice as long as a regular Thalys) brings you with a speed of close to 300Km/hr in 2Hr30min some 515Km further to Osaka. The seminar in Osaka was hosted and organized in cooperation with the OCCI (Osaka Chamber of Commerce & Industry). Also here the seminar was very well attended by 46 participants of local companies.



Q-Star Test nv adds Kingsly Instrumentation and Communication Pvt. Ltd (KICPL) as India Distributor

Q-Star Test also announces that Kingsly Instrumentation and Communication Pvt. Ltd (KICPL), an Indian Company engaged in providing Test & Measurement and Data Conversion solutions, has become a distributor of Q-Star Test products. The agreement extends sales and technology support for Q-Star's technology solutions throughout India.

KICPL based in Bangalore, India represents various global Companies providing advanced Test & Measurement

About KICPL

KICPL was incorporated in 1993 to provide quality Test & Measuring Instruments to the Indian Industry. Over the Company has added quality products from leaders in the Industry to service the needs of the Indian customers. KICPL specializes in providing Test Instruments, Data Convertors (A/D, D/A & DIO), Data Recorders and Data Analysis Software. Some of the key customers include leading Semiconductor Design / Test houses, Public Sector Undertakings, Government Labs and MNC's.

About Q-Star Test

Q-Star Test was founded in 2000 by Dr. Hans Manhaeve, an award-winning Researcher from IMEC, the renowned European Microelectronics Research Centre. The firm produces high-speed, high-accuracy precision current measurement modules that work in conjunction with Automated Test Equipment (ATE) as provided by Teradyne, Verigy and LTX/ Credence to greatly reduce production test times while improving test and product quality. The firm has expanded over the years and recently forged collaboration agreements with key firms in the USA, Japan and Taiwan.

products and Data Converter products. The Test & Measuring Instruments are used to measure and characterize various defects in electronics circuits and make advanced measurements that aid in faster design turnaround. The Data Converter products are used in ATE / Customized Systems where measurement throughput and faster processing is critical.

Sheik Ahmed, KICPL's Director said, "Our 16 years experience in supplying quality T & M equipment to various Industries in general and semiconductor design/ test houses in particular will help us in providing quality products that will help the semiconductor industry achieve faster results thereby improving overall quality and reliability of their products. We believe that Q-Star's products will provide our customers with the right tools for overall quality improvement of their products."

According to Q-Star Test's CEO Hans Manhaeve, "We are pleased to team with KICPL to offer more value to our customers and to extend our customer base providing solutions that help to built better electronic circuits at lower costs. With over 600 of our instruments sold worldwide (USA, Europe and Asia) that are used for critical test applications, the partnership with KICPL allows to expand our activities in the Far East and India in particular."

Both seminars were very well appreciated by the audience. Overall around 90% of the attendants were satisfied with the quality of the seminars.

If we look a layer deeper most seminar participants were interested in foreign markets, in particular, for technology cooperation / R&D and information gathering.



This is obviously good news for a technology network like DSP Valley which has internationalization as a main objective.

Later that week (from 12 till 14 May) the DSP Valley delegation with Altreonic, AnSem, NXP Semiconductors and Target Compiler Technologies could be visited at the ESEC Embedded Systems exhibition at the "TOKYO BIG SIGHT" conference center East 5 Hall 34-8. The exhibition attracted over the three days in total 122.371 visitors, almost 10.000 more if compared to 2009.

More important is that all DSP Valley exhibitors had very interesting conversations and good interaction with the visitors. New for

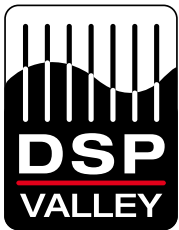


2010 was that also TV-media covered our presence at the ESEC show, see picture above of Dirk Deruyver from FIT giving an interview in Japanese.



Exploring the IC ecosystem in DSP Valley

On Wednesday, May 26, 2010 DSP Valley and imec organized a technical seminar at the premises of imec in Leuven. The goal of the seminar was to give an overview of the expertise available in the DSP Valley network on IC design and to show by real cases how collaboration with these local partners can help your company. Some 60 people registered for this seminar in which experts from (fabless) design houses and product manufacturers shared their expertise and experiences.



The first speaker of the seminar was Stefan Gogaert, CEO of AnSem, who gave an overview of the semiconductor industry value chain in a changing

world. He highlighted the change in the business models. Starting in the beginning of the 1950's with Integrated Device Manufacturers (IDM) over fabless design houses we now see emerging a new model called Value Chain Producer (VCP) which is a company that collaborates with foundries, IP and service providers, EDA suppliers, package, assembly and test operations in designing and producing chips. Peter Simkens from DSP Valley showed that a lot of the different steps in the complete value chain are actually available in the DSP Valley network.

Bruno Bougard started with an overview of the GNSS receivers developed at Septentrio: from the first breadboard to the very last product as the AsteRx3 and he further elaborated on their IC design activities. IC integration is a must and Septentrio, as an IMEC spin-off, therefore collaborates with several DSP valley members. He stressed that because of the increasing complexity of the product they have to use state-of-art technology. Their product volume is too low to keep on scaling but the volume is too high for FPGA. So it is always a difficult but challenging exercise when designing a next product generation. Ramses Valvekens, CEO of Easics and one of Septentrio's partners, gave a useful comparison between the use of an FPGA and an ASIC. He gave some topics in a kind of checklist to take into account to

help one make the decision. He elaborated also shortly on the importance of a solid design flow.

Johan Van Ginderdeuren from NXP Semiconductors, illustrated DSP Valley's open innovation setting with the ultra low power CoolFlux DSP cores. Frederic Stubbe from Essensium explained on a project where the CoolFlux core had been integrated in a customer's project.

Richard Visée showed how his company, SystematIC Design, sees opportunities for SMEs and other companies through integration. He illustrated that with three cases they have done in the past where the annual number of ICs is rather low. Although there is a tendency to digital implementation of electronic functions, the world is analog and therefore he advised to use the best of both worlds! In his vision the design preferably starts with a high level specification without the bias of a predetermined solution. He also advised not to make unnecessary choices that will set boundaries in an early phase since you may regret this later.

After the coffee break, Bram De Muer, CEO of ICsense, gave a presentation where he elaborated on a low cost sensing solution developed with DSP Valley partners from idea to final product. He concluded his talk with the advice to the audience not to be scared to start with IC development since it is within reach and the complete state-of-the-art ASIC development is possible with partners within in the region.

Tom Van Assche, ASIC project leader at Cochlear Technology Centre Europe, explained why custom ASIC design is important for his company. The three

driving factors for a hearing implant are Performance, Size and Power. Of course Moore's law helps but for Ultra Low Power design a holistic approach is needed, i.e. focus on all levels of the design: system, algorithm, architecture, circuit and technology. To find the right balance between the three factors an iterative process is needed. In this way their custom ASIC has superior results compared to other general purpose processors when it comes to DSP benchmarks. Tim Morlion then gave an overview of the ASIC methodology and design tools used by Easics.

To conclude the talks, Thierry Watteyne, CEO of Barco Silex, strongly said "yes" to the question he posed in the beginning of his talk if IC design in Belgium by use of a local ecosystem still makes sense in this complex semiconductor industry. And this is not only true for mixed signal ICs (More than Moore) but also for complex digital SoCs (More of Moore). His company is able to provide local players with complex and competitive SoC solutions thanks to advanced competence and experience in key aspects of SoC development and thanks to close and proven partnership and collaboration with key players in IC manufacturing. He illustrated this with a project in which they have developed a hardware platform for payment terminal in which IP re-use, application specific IP development, power management, verification&validation methodology and risk management where key aspects for the SoC development.

During the coffee break and the networking drink afterwards four companies showed demos to the participants and had the opportunity to network with the participants. Positive feedback from the speakers and exhibitors prove that these networking moments are very valuable in matchmaking companies with each other. If you are interested in future technical seminars or want to know more on the DSP Valley IC ecosystem then please contact Peter Simkens who will be happy to help in finding partners. ■

AUTOSAR seminar

Karel de Grote University College
September 14, 2010

Software content in vehicles has grown steadily over the years. The amount of code present in even low-end vehicles is going towards 100 million lines of code. An increasing amount of this automotive embedded software and the related automotive networking is being developed

according to the AUTOSAR-standards. But what is AUTOSAR actually? And how does it help to control cost and automotive-grade quality? How can AUTOSAR be of any use to the SMEs or to suppliers? These and other AUTOSAR-related topics will be discovered during a one-day seminar, organized by TERA-Labs (Karel de Grote University College), Flanders' DRIVE and DSP Valley.

Venue:

Karel de Grote University College
 Campus Don Bosco Hoboken
 Salesianenlaan 30
 2660 Hoboken
 Belgium



www.teralabs.org

Academia to Business Forum (A2B) 2010

IBBT, Gent, Belgium
September 23, 2010

On September 23rd, 2010 DSP Valley and IBBT organize the yearly A2B-forum, a forum where research institutes, universities and university colleges will present research projects to the industry. The focus of the projects is on hardware and embedded software related topics. The goal of this half-day forum is two-fold. On the one hand, the academic partners will present the research project to a broad audience and in that way they have the opportunity to extend the user committee of the project and they

can exchange ideas for new projects. On the other hand, companies will get an overview of the research projects on embedded technology in the DSP Valley activity region and they will be able to get first-hand information of the specific projects. During and after the presentations there will be plenty of opportunity to have private discussions with the researchers. During the whole event there will be a "Café Embarqué" where the visitors can visit the demos and poster booths. We will provide time and opportunity to network with the different participants and presenters to allow discussions on details.

The complete program details are available on our website:
<http://www.dspvalley.com>

The presentations will be given in Dutch.

For more information please contact
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www.dspvalley.com

Seminar: High-Level Synthesis tools - an overview

Campus De Nayer, Lessius, Belgium
September 28, 2010

The capacity of silicon doubles every two year, according to Moore's law, resulting in digital designs with an ever growing complexity. Traditional hardware design at Register Transfer Level (RTL), written by hand using a hardware description language (HDL), becomes too time-consuming.

High-levels synthesis (HLS) uses methods and tools in order to raise the design productivity and quality. The design entry starts from specifications

at a higher level of abstraction (algorithmic / behavioral), independent of the RTL-architecture, which allows a better management of the system design complexity. HLS tools automatically generate verified RTL-architectures that are optimized to various design implementation options (area, performance, power), improving the quality of the result and reducing the overall design cycle.

In the Fast-ProMoCo project (IWT-TETRA), commercial HLS-tools were evaluated based on common criteria: learning curve, level of abstraction, verification time, capabilities and efficiency

of the synthesis process. Demonstrators were built for the same test-case. During this seminar the results of the Fast-ProMoCo project will be described, vendors of HLS-tools present their products, designers will share their experience.



<http://www.fast-promoco.be/>

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Business-to-Business Forum 2010

www.dspvalley.com

**Sportoase, Leuven, Belgium
October 26, 2010**



Mark the 26th of October 2010 in your agenda! On that Tuesday, DSP Valley expects you on the yearly B2B Forum.

This time the venue for this outstanding matchmaking event will be the Sportoase in the city center of Leuven, Belgium.

An entire day filled with interesting face-to-face meetings with some of the leading figures of the embedded industry in the BeNeLux and Europe that is

for the ninth time in a row the simple but effective format of this matchmaking event. Prior to the event, a list of participating companies will appear on the DSP Valley website. If you decide to enroll, your name will be added to this list. A few days before the actual B2B Forum, you can send in your list of preferred contacts and DSP Valley will try to create a suitable schedule.

As every year, the technology focus for this matchmaking forum will be on "Design of embedded technology and systems for signal processing". This includes image processing, sound

processing, communication and navigation technologies. The development of these technologies covers as well the (micro-electronics) hardware as the (embedded) software, as well digital as analog and mixed-signal as sensor-technologies.

All the information will appear soon on the DSP Valley website. If you are interested in participating in this matchmaking event, send your coordinates to vera.geboers@dspvalley.com and you will be kept up-to-date with all practical info.

Contact Information

DECT ULP drives acceptance of wireless sensor networks • p.1

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Altreonic's StarFish scalable high reliability controller available for preview • p.2

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Six VUB excellence centers for strategic research – privileged partners for innovation and projects together with industry • p.4

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Previewing C vAnalyst Parallelization Features with vLabs • p.4

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Verum and Solidsource close technology partnership agreement • p.6

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AnSem offers a complete development package for SerDes • p.6

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Sigasi announces first round funding • p.7

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Q-Star Test and BEST-IIC announce a strategic cooperation • p.8

Q-Star Test nv adds Kingsly Instrumentation and Communication Pvt. Ltd (KICPL) as India Distributor • p.9

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DSP Valley visit to Japan • p.8

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