

newsletter

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Byte Paradigm, new member of DSP Valley

Byte Paradigm, a company based in Nivelles (Thines, Belgium), develops innovative PC-based instruments to test and debug embedded systems.

Founded in 2005 by a team of 3 electronic engineers specialized in digital ASIC, SoC, FPGA and board design, Byte Paradigm has developed a comprehensive range of instrumentation products that includes digital pattern generators, SPI and I²C master and ana-



lyzers. Byte Paradigm's PC instruments are used today in companies like RF Micro Devices, Intel, Texas Instruments,

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IBM, Infineon, ST Microelectronics, CSR, ABB, Huawei - to name a few.

Byte Paradigm's growth is due to several key elements.

First, Byte Paradigm has established durable relationships with key customers for the design of custom electronic systems. Byte Paradigm is specialized in high-speed digital board design (up to 800 MHz digital) that use high end FPGA and multi-gigabit links for the transfer and process-

ing of digital data. This activity – which Byte Paradigm is still sustaining – is an important source of funding and experience that Byte Paradigm leverages in its own range of products.

Second, the large experience of Byte Paradigm's crew in FPGA, ASIC, SoC and other system design flows allows us to constantly listen to our potential customers' needs and target application niches for test and debug instruments.

Finally, Byte Paradigm sales benefit from a worldwide network of distribution partners. Together with a strong web presence, this considerably extended the grasp of Byte Paradigm over its market, while maintaining a lightweight struc-

ture. Today, Byte Paradigm is present in USA, Germany, France, UK, Israel, China, Taiwan, South Korea and in talks with other partners, notably in Japan.

Byte Paradigm is dedicating a lot of its resources to R&D and is going to launch several new products in 2010 and 2011. This innovative offering poses a lot of exciting challenges to our company. It requires from us to explore new forms of partnerships. At Byte Paradigm, we are convinced that being a member of DSP Valley will allow us to leverage the resources located in our direct environment in order to better understand our target customers' need and, in the end design better products for them. ■

Are Regions a Driving Force for Innovation?

Preface

Subsidies are a classical tool to foster R&D and innovation in many high tech domains, including (embedded) ICT and semiconductors. However, other possibilities exist for driving the innovation, such as venture capital, public procurement, etc.

Regional clustering is another tool for fostering R&D and innovation. To start with, clusters bring together industrial companies and/or research organizations, complementing each other with their technologies, competencies and skills, and thus creating a very interesting value chain for the participants. One of the aspects for having a successful cluster is proximity: for the cluster participants it is easier to cooperate if they can find each other just next door. This automatically means that clusters very often have a regional dimension. The benefit for the cluster members is the regional availability of the technologies, skills and services missing in their own organization; moreover they can find basic know-how by networking with the local/regional universities and other research institutes.

DSP Valley is a good example of such a regional cluster: with a well defined technology focus of embedded systems and semiconductors, the region from Leuven

to Eindhoven clusters a wide variety of industrial and academic organizations, each with their own specialization, and very complementary to each other. By creating critical mass in R&D excellence, and by connecting the best to the best, DSP Valley creates a strong ecosystem and value chain in embedded software development and micro/nano-electronics hardware design. In the DSP Valley cluster, the value chain is built by a lot of strategic partnerships by the cluster members.

DSP Valley is also a good example how a regional cluster can promote internationalization activities for the local companies (especially SMEs) lacking internal resources. Indeed, DSP Valley participates with member delegations in international events such as technology exhibitions and road shows. Moreover, by operating in the region extending from Leuven in Belgium to Eindhoven in the Netherlands, DSP Valley is also a good illustration of the creation of a cross-border world class cluster, involving key players from both sides of the border, such as IMEC, Philips, NXP, Jabil, Barco etc.

Finally, not all competencies are reachable at regional level. Therefore, the DSP Valley cluster is also partnering with other European clusters, in embedded

systems or semiconductors, to widen the partnering horizon of its members. The same principle of working together between regional centers of excellence is also embraced by the recently founded Knowledge Information Centers (KICs) of the European Institute of Technology (EIT).

Nevertheless, regional clustering still has important challenges. Can we identify common interests of regions in embedded systems and semiconductors to better link the regional and European R&D and innovation policies? Can we stimulate a better and more coordinated use of available funding instruments? But the most important challenge is: how can we make use of ALL resources? How can we involve all key actors along the value chain, including end-users such as public authorities, in the development of new technologies?

DSP Valley is constantly at the forefront to tackle these challenges. However, we can not solve these challenges on our own. A coordinated approach with other regional clusters is the only way to go. ■

Peter Simkens
Managing Director
DSP Valley



Leuven's imec and ICsense partner in European cancer lab-on-chip project

European research institute imec (Leuven, Belgium) and its project partners, among which the Leuven-based mixed-signal IC design house ICsense, have launched a European collaborative research project to build a lab-on-a-chip for the detection of tumor cells in blood.



The Miracle project (Magnetic Isolation and molecular Analysis of single Circulating and disseminated tumor cells on chip) is due to run for four years from Sept. 1 2010 and the partners are set to receive €7 million (about \$9 million) towards a total budget of €9.18 million (about \$11.8 million).

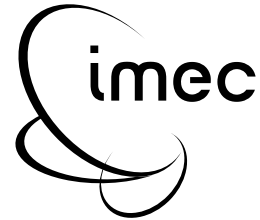
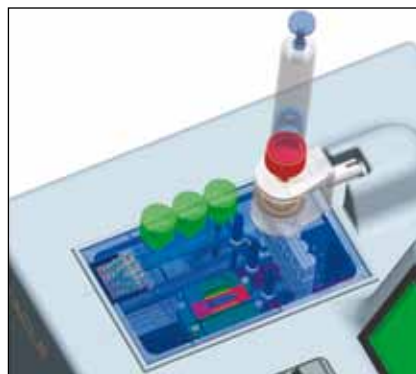
The creation of a microfluidic device able to isolate and detect circulating and disseminated tumor cells (CTCs and DTCs) in blood is a step towards faster and more cost-efficient diagnosis of cancer. The Miracle project aims at developing a fully automated and integrated microsystem to provide the genotype of CTCs and DTCs starting from clinical samples.

In a preceding joint project called Mascot, individual microfluidic modules for cell isolation, cell counting, DNA amplification and detection were developed. Based on this expertise and strengthened by additional partners, the development of a fully automated, lab-

on-chip platform to isolate, count and genotype CTCs is envisaged within the framework of the Miracle project.

For genotyping, genetic material, such as a mitochondrial RNA, will be extracted from the cells and multiple cancer related markers will be amplified based on multiplex ligation-dependent probe amplification followed by their detection using an array of electrochemical sensors.

Imec is project coordinator and is collaborating with the Universitat Rovira I Virgili (Spain), the Institut für Mikrotechnik Mainz, AdnaGen, ThinXXs and Consultech (Germany), MRC Holland (The Netherlands), the Oslo University Hospital (Norway), the KTH Royal Institute of Technology, Multi-D and Fujirebio Diagnostics (Sweden), the European Cancer Organization and ICsense (Belgium) and Labman (UK). ICsense will be responsible for the design of the IC for cancer cell detection and characterization through impedance spectroscopy. ■



About ICsense

ICsense is an ISO 9001:2000 certified IC design house, based in Leuven, Belgium, offering IC design services and ASIC turnkey solutions. The core business of ICsense is high-performance analog, mixed-signal and high-voltage integrated circuit design. ICsense has a key competence in sensor, actuator and MEMS interfaces, data-acquisition, power/battery management and high-voltage IC design. ICsense has a technical team of 25 engineers. ICsense is the preferred partner of several international companies, located in the Europe, the US and Canada, Australia and Japan.

About imec

Imec performs world-leading research in nanoelectronics. Imec leverages its scientific knowledge with the innovative power of its global partnerships in ICT, healthcare and energy. Imec delivers industry-relevant technology solutions. In a unique high-tech environment, its international top talent is committed to providing the building blocks for a better life in a sustainable society. Imec is headquartered in Leuven, Belgium, and has offices in Belgium, the Netherlands, Taiwan, US, China and Japan. Its staff of more than 1,750 people includes over 550 industrial residents and guest researchers. In 2009, imec's revenue (P&L) was 275 million euro.

“Nosey Elephant Studios” - Audiovisual laboratory for research and industrial applications



Vrije Universiteit Brussel

Nosey Elephant Studios is a new audiovisual laboratory part of the infrastructure of the Department of Electronics and Informatics of Vrije Universiteit Brussel (ETRO). The lab is operating as a service provider in audiovisual content creation in the fields of speech/audio and video processing, audiovisual behavior analysis, speech emotion recognition and synthesis and film/TV post-production. Research groups active in these fields can use the facility in order to capture audiovisual data optimized for their projects, in controlled environment (acoustic and lightning conditions) using state-of-art equipment.

At the same time, Nosey Elephant Studios operates as a platform for tech-

nology transfer, valorizing the results of research produced at ETRO and investigating ways of offering them as services.

A technology that is currently available at Nosey Elephant Studios/Movies is a system for automatic dialogue replacement (ADR). During post-production of soundtracks for film, video and television series, it is often necessary or desirable to replace the original actors' dialogues that were recorded live on the film set by re-recorded studio dialogues, because the original location recordings might for example be distorted by some kind of background noise that is difficult to control. This dialogue replacement introduces a lot of mismatches between the lip movements that the audience

perceives and the actual speech sounds they hear. Our system allows to automatically edit a studio soundtrack, measure its timing relationship with the original reference soundtrack and compensate for the lip-synch errors by time-scaling the studio soundtrack, such that the synthesized output signal precisely synchronizes with the lip movements in the picture. This ADR system is the result of many years of research of the ETRO based DSSP research group. More info and demos can be found here: <http://www.etro.vub.ac.be/Research/DSSP/DEMO/ADR/>

Nosey Elephant Studios/Multimedia is providing all the infrastructure and engineering of a professional grade record-



Altreonic's scalable and formalized technology gives more for less.

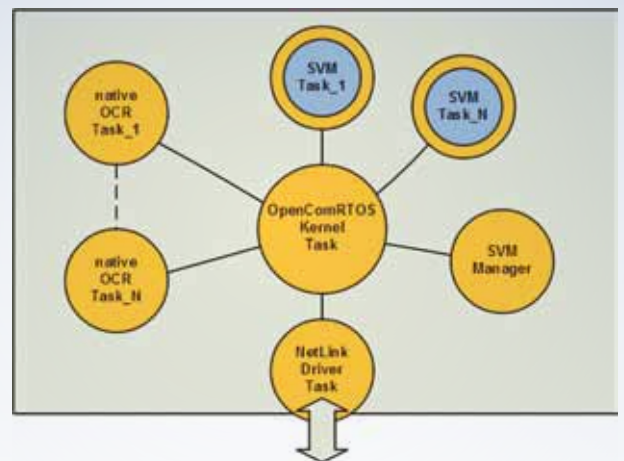
Altreonic is now announcing two new products that clearly demonstrate how a formalized development can result in more scalability and less energy consumption. A formalized development is more than verifying correctness; it actually results in cleaner, more efficient and more scalable architectures.



Virtual Machine for C in 3.8 KBytes

A first example is Altreonic's novel **Safe Virtual Machine for C (SVM)**. Tuned to the needs of embedded systems it allows to dynamically download C compiled binary code to OpenComRTOS nodes independently of the target processor. Yet, the Virtual machine only requires **3.8 Kbytes of program memory** (measured on an ARM Cortex M3). Every processing node in an OpenComRTOS supported system can host multiple Safe Virtual Machine tasks, each of which can use the native kernel

services and hence communicate system wide. SVM tasks can also be unloaded, updated at runtime as well as moved between networked OpenComRTOS nodes. For safety purposes the Virtual Machine can verify memory accesses and catch boundary violations and numerical exceptions at runtime.



Other OpenComRTOS nodes

ing studio for the production of audiovisual databases. Multimodal audio-visual signal processing (in-synchrony processing of multiple audio and video signals) is an emerging research area, where data obtained through microphones and cameras are used in order to develop, train and test new multimedia applications. The audiovisual recording system installed in its full deployment can capture up to 6 SD/HD SDI video streams and 24 audio channels. All these data are captured in uncompressed format and can be distributed in a desired compressed format. Nosey Elephant Studios is producing databases for the technologies being developed at ETRO, like microphone arrays, 3D surround sound, audiovisual photorealistic text-to-speech synthesis and emotional and expressive speech synthesis and recognition. In conjunction with other departments, researchers are using this facility to explore human behavior analysis, studying mother-child communication or ways of enriching the interaction between humans and robots. In addition, researchers can test their algorithms using microphones, loudspeakers or video cameras under variable acoustic and lightning conditions.

Together with the Department of Culture of VUB, Nosey Elephant Studios/Music is investigating an application for real time video streaming of live music events, through wireless networks, on mobile devices. Nosey Elephant Studios/Music also provides music production services for musicians or bands (www.myspace.com/noseyelephantstudios).

Nosey Elephant Studios can also be hired by external customers for research or industrial projects. ■



Recording room



Control room

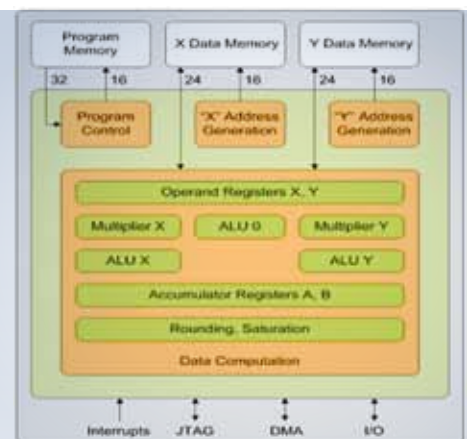
As the VM is based on the ARM Thumb2 instruction set, it is also possible to execute the binary images in native mode on most of the ARM processors. While VM tasks execute slower than native code, the performance is adequate given the intended range of applications. Typical applications for the SVM are remote diagnostics, fail safe, fault tolerant control, and processor independent programming.

Full OpenComRTOS on CoolFlux DSP in just 2 Kwords.

A second example is the **port of OpenComRTOS to the ultra low power CoolFlux DSP** core of NXP. A full kernel with all services only requires about 2 Kwords for program memory and less than 1 Kwords of data memory. Nevertheless, this is still a complete priority based preemptive scheduling RTOS.

Besides task scheduling, services provided are events, semaphores, resources, port hubs, fifos, packet and memory pools in blocking, non blocking, blocking with timeout and asynchronous semantics. Porting on CoolFlux DSP has been swift and efficient thanks to the excellent C-language support from the CoolFlux DSP tools originating from Target Compiler Technologies.

For applications where power consumption is paramount, using less memory means higher performance and less energy consumption. With OpenComRTOS, this is a result of the formalized development resulting in a very clean architecture. In addition, with OpenComRTOS one can transparently use a multicore architecture allowing to distribute the application. If this allows to reduce the clock frequency, thus even more power can be saved.



The OpenComRTOS suite consist of the high level visual development environment (OpenVE) in which the user specifies applications and target topology in an independent way allowing to simulate the application on his development PC. Code generators than generate most of the target specific C code and the buildsystem. A new task level debugger and the visual OpenTracer allow examining and profiling the application at runtime. ■

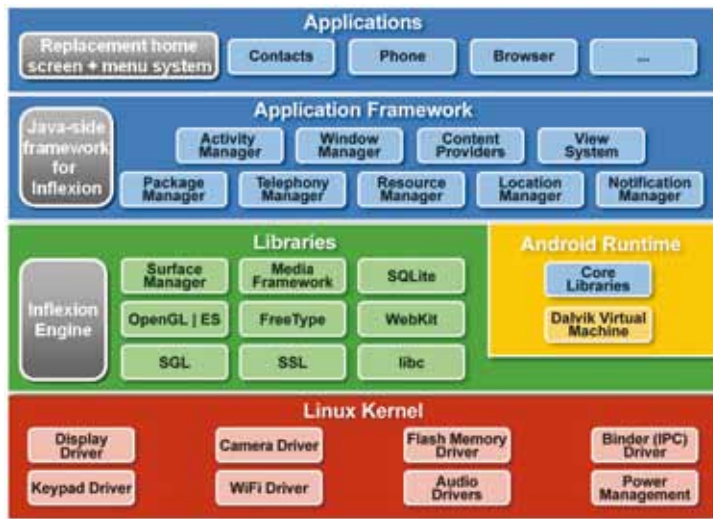
Enabling GUI Differentiation on Android Devices

By Phil Burr, Embedded Software Division of Mentor Graphics



The Android development platform enables embedded device manufacturers to quickly develop products in a variety of vertical markets. But standardizing on a single technology could prohibit product differentiation and functionality. A device's graphical user interface (GUI) is the most obvious and cost-effective way to differentiate an Android-based device, but without the right tools, UI customization requires significant engineering resources.

devices. This solution delivers a distinctive look and feel to any Android product without requiring the developer to understand low-level graphics APIs, or modify applications at the code level.



Mentor's Inflexion UI within the Android software stack.

Design teams can create stunning new application launchers and "home screens" for Android by using a visual drag and drop method. Developers can avoid writing or modifying a single line of UI code to achieve this. Rich visuals, including 3D animation, lighting and Open GL/ES 2.0 effects, are employed within minutes.

The Inflexion UI Engine is optimized for Android's built-in 3D OpenGL/ES API. This "engine" sits alongside other system libraries (see Figure) and interfaces to the OpenGL/ES library for 3D rendering. Moving to the Application Framework, the functionality of the Inflexion Engine is exposed for Java applications. At the top level, Inflexion comes with a 'shell application' to replace the standard Android home screen and menuing system. It includes comprehensive documentation and examples showing how Inflexion can be used to create stunning UIs for any application.

The ability to make significant and compelling changes to Android (completely changing the "look and feel" of a menu system, adding advanced UI effects), requires many man years of software coding. It also results in a UI which is hard-coded and thus difficult to update or adapt to different markets. An alternative approach is to use a GUI tool and a graphics engine which enables software engineers, GUI designers, and content providers, to rapidly create, customize, and test GUIs independent to the actual Android software.

An ideal GUI tool and engine would remove the need to write code at the UI level, allowing software engineers to focus on the underlying application functionality, significantly reducing both resource and project risk. The ideal tool and engine would also separate the UI from the underlying application logic, allowing UIs to be modified without changing the application code. This separation is critical for providing the best possible UI experience and best exploiting the device's silicon (e.g. OpenGL/ES 2.0 accelerated 3D).

Application content is managed by Inflexion software modules that serve as data providers to the device's user interface. Thus, Inflexion maintains a clear separation between presentation and content. This proven concept enables completely new interface designs without programming or scripting because it automates the key interactive UI behaviors such as hierarchical browsing and scrolling, plus the ability to include rich animations common to a wide range of UIs. This GUI technology makes it easy for Android device makers to master a compelling, distinctive, and easy-to-use GUI which is critical for any Android-enabled device.

A GUI tool and graphics engine allows the design team to package their designs into templates and themes for rapid deployment on the Android platform, regardless of whether it's running on the physical target device or on the Qemu emulator (in the Android SDK). The ideal tool enhances graphical elements quickly (such as bitmaps, icons, menu items, and other UI components) while the code remains untouched.

Menus can be easily structured around the chosen design paradigm (for example, carousel, widget screens, etc.) and embedded widgets, can be updated with live data feeds. Applying this level of customization to a home screen allows the OEM to develop a highly differentiated offering.

A GUI tool and engine for Android, known as Inflexion™ UI from Mentor Graphics is available for Android-based

A Euro-Brazilian consortium to tackle the threat of Ionospheric Scintillation to GNSS operations in Latin America



The European Galileo R&D Framework Programme (FP7) and the European GNSS Supervisory Authority (GSA) granted co-funding to the CIGALA Consortium (<http://www.fp7cigala.eu>), lead by Septentrio, aiming to develop and test receiver-level ionospheric scintillation mitigation to increase the robustness of professional multi-frequency GNSS based applications in low latitude regions, in particular in Latin America.

Solar induced ionosphere activity may lead to the scintillation of the GNSS signals that can not only degrade signal quality but also cause signal outage, therefore posing a major threat to GNSS applications demanding high levels of accuracy, availability and integrity. The problem is particularly acute in low latitude areas and will be exacerbated with the next solar maximum, predicted for 2013. Latin America relies to a great extent on GNSS in support of activities

such as land and offshore surveying, and therefore is particularly exposed. This was demonstrated during latest major solar storm in 2003, which led to very costly delays and cancellations of major surveying and drilling operations as well as serious disruption of the WAAS system in those areas.

To tackle the challenges posed by the next solar max, a Euro-Brazilian consortium led by Septentrio (BE) and including the University of Nottingham (UK), INGV (IT), Pildo Labs (SP) and Brazilian partners Petrobras, Universidade Estadual Paulista "Julio de Mesquita Filho" (UNESP) and Consultgel was established to pursue collaborative research.

The project comprises scintillation climatology research, signal propagation and tracking R&D as well as a large scale ionospheric measurement and test campaign that will be conducted in Brazil with the support of several local academic and industrial partners, including Petrobras.

"With the currently increasing solar

activity combined with a reliance on GNSS based technologies that has never been so high, robustness to ionospheric disturbances will be crucial to the Latin American market" said Peter Grognaard, Managing Director of Septentrio. *"CIGALA receiver-level scintillation countermeasures will strengthen Septentrio's receivers capability to deliver the required accuracy even in presence of moderated to strong scintillation."*

"CIGALA technical results are expected to significantly advance the state-of-the-art in understanding climatologic, signal perturbation and tracking dynamics aspects of strong ionospheric scintillation events." said Prof. Joao Francisco Galera Monico, Associate Professor at UNESP. *"The CIGALA project will leverage research and development activities coordinated between European and Brazilian experts, involving most affected local GNSS users to promote greater awareness of the problem and solutions proposed by Septentrio"*

Sigasi announces its University Program

Sigasi launched its University Program in August at the Conference on Field Programmable Logic (FPL) in Milan, Italy. Through this Program, both teachers and students can use Sigasi's software free of charge for their educational purposes.

When students get to their first hardware designs, most have already taken at least one programming course. In these courses, students usually work with IDEs (Integrated Development Environment) like Eclipse or Visual Studio. Since Sigasi HDT (Hardware Development Toolkit) is an IDE built on top of the same technology, students can work in a familiar environment. Autocomplete, context hovers, quick fixes and code navigation are all immediately and seamlessly at their dis-

posal. Using all of these familiar features, they can concentrate on learning new engineering skills and concepts instead of struggling with the tools. The net result: better graduates and satisfied professors.

Sigasi wants to reach out to the entire academic community. Today, students and teachers from almost one hundred universities, schools and colleges in over thirty countries are using Sigasi's HDT, free of charge. Signing up for an edu-



Sigasi
automated hardware refactoring

cational license is just a couple of clicks away on Sigasi's website (www.sigasi.com). Apply for a license now and experience the future.

Barco presents innovative solution for sub-frame latency processing of single-tile JPEG 2000 images

Barco Silex, Barco’s center of embedded video coding, has presented a new JPEG 2000 IP core which performs at sub-frame latency while preserving the high quality of single tile images. Thanks to these new cores, the cumulated latency delay to encode and decode an image becomes less than 1 frame. In the case of HD application, the total delay can be as low as 10ms.



“Within the image processing industry, everybody is looking for ways to reduce the latency of its system, but some applications just can’t afford the delay introduced by usual codec solutions,” says Thierry Pauwels, Application Engineer at Barco Silex. “We are therefore excited to present these new IP cores, as they offer a unique solution to maintain the high quality of single-tile JPEG 2000 images with sub-frame latency.”

Similar to the other IP cores from Barco Silex, the new cores are based on a portable and flexible architecture that can be tuned to the specific needs of each application. The low-latency solution supports major vendors of FPGA platforms to provide customers with the most appropriate single-chip solution.

Barco’s latest solution will improve the processing performance of broadcast professionals, but it is also very well suited for other markets that require low-latency codecs, such as surveillance, medical or other industrial applications where a high level of image quality is expected. ■

Reference	Specifications	Performance
BA129	Sub-frame latency JPEG 2000 decoder Complete JPEG 2000 decoding solution for low latency video Single tile images up to 4K, 2K, 1080p and 1080i, 720p, ... XYZ, RGB, YUV (4:4:4 or 4:2:2) color spaces Up to 12 bits per color component	1080i@180fps 1080p@60fps 2K@48fps 4K@24fps
BA130	Sub-frame latency JPEG 2000 encoder Complete JPEG 2000 encoding solution for low latency video Single tile images up to 4K, 2K, 1080p and 1080i, 720p, ... XYZ, RGB, YUV (4:4:4 or 4:2:2) color spaces Up to 12 bits per color component Flexible optimal rate allocation	1080i@180fps 1080p@60fps 2K@48fps 4K@24fps

Technical features

- Single FPGA solution for sub-frame latency:
 - <10ms total latency delay for encode + decode
- Complete image processing (no tiling):
 - HD: 720p30/60, 1080i, 1080p30/60
 - Digital Cinema: 2K, 4K
 - Custom frame sizes up to 8K or larger
- Customizable output bit rate: up to 200Mbps / 400Mbps / 800Mbps / 1+ Gbps
- XYZ, RGB, YUV (4:4:4 or 4:2:2) color spaces with support for ICT/RCT color transform
- Supported encoder parameters:
 - Wavelet filters: 9/7 and 5/3
 - Pixel depth: up to 12 bits per color sample
 - Configurable bit rate on a frame by frame basis with 3 selectable regulation modes
 - Quality: quantification, weights, ...
- Minimal user intervention
- Fully synchronous design

About Barco Silex

Barco Silex is a leader in contract engineering services, custom hardware and software development, as well as Intellectual Property (IP). Its high quality JPEG 2000 IP cores, developed since 2002, are optimized for all leading-edge FPGAs as well as for legacy platforms. Thanks to its continued stream of aggressive innovations, Barco Silex stays ahead of the competition. Barco Silex’s history as a custom electronic design house (ASIC, FPGA, DSP, Board) specialized in video coding, cryptography, security and memory controllers goes back to 1991, offering the best guarantee for continuous support throughout the complete lifecycle of products.



New offices for Ir.deto

Ir.deto has nearly tripled its workforce and grown its revenue by over 35 percent annually over the last four years, and continues to invest in products and people that will make future growth possible. To accommodate this growth and expansion, Ir.deto has invested in building a new Western Headquarters in The Netherlands while its dual headquarters in Beijing, China signifies its ongoing commitment to the East.

Ir.deto's new headquarters is designed to enable a new way of working that embraces environmental responsibility while delivering economic benefits. With more employees balancing working hours among the home, office and other external locations, the new building caters for 70 percent of the workforce in the office at any one time. Moving away from individual designated workspaces, the open plan office provides a wide variety of work areas, allowing staff to choose the space that best suits the type of work they are engaged in at the time

and promoting collaboration and the consistent flow of ideas and information. Ir.deto's worldwide Clean Desk policy, which aspires toward the ideal of a paper free environment, was originally trialed in Beijing and is also now in full operation in Hoofddorp.

The new headquarters includes IT solutions that reduce the need for travel, such as audio and video conferencing technologies, and save on equipment and power. Environmental infrastructure includes a heat and air conditioning system housed 80 meters below ground that stores hot and cold water, reducing the energy needed to heat and cool the building in the winter and summer months. Sensors are also utilized in temporary used areas such as bathrooms and meeting rooms to control lighting, further minimizing energy usage.

The building itself was designed using



green architectural principles and is constructed from 100 percent sustainable wood, with carpets and wall coverings made from recycled materials. It is built opposite a train station and includes bike racks and showers to encourage employees to use environmentally friendly modes of transportation.

The Hoofddorp headquarters is the flagship location for Ir.deto's new way of working, while the Beijing headquarters is currently finishing a similar transition. With additional hub offices in strategic North American geographies like Carlsbad, Calif. and Ottawa, Ir.deto has changed the genetic makeup of the company and is able to act upon and support customers regardless of where they are in the world. ■

Access to TSMC technologies through leading European partners: imec and DELTA partner to provide comprehensive ASIC solutions

Imec, certified TSMC Value Chain Aggregator (VCA), and DELTA Microelectronics, a leading provider of ASIC services, have concluded a cooperation agreement to provide customers in Europe, the Middle East and Africa (EMEA) with comprehensive TSMC-based turnkey and partial turnkey ASIC services.

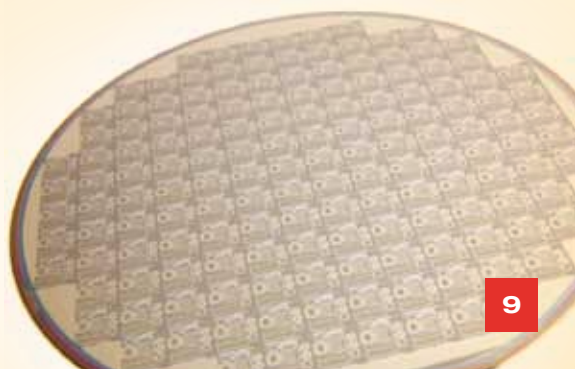
This agreement combines the strengths of these two recognised players in the EMEA microelectronics industry. Imec as certified TSMC Value Chain Aggregator (VCA) provides Customer-Owned Tooling (COT) services including TSMC wafer supply, access to TSMC technology and production information, library licenses, design support, GDSII submission, and preparation for production. Building on these services DELTA offers ASIC related turnkey and partial turnkey solutions including prototyping, package development, assembly, test, qualifications, characterization, failure analysis, logistics and supply chain management.

"This partnership is unique in Europe and provides customers with the most comprehensive and reliable path to successful ASIC development and production using TSMC technologies. It combines the strengths and long track record of imec and DELTA", commented Per Ølund, Director of DELTA Microelectronics.

"With the combined strengths of both organizations, customers in EMEA can benefit from the experienced teams at imec and DELTA with local and same time zone support for their TSMC based ASIC projects. This will reduce risk and shorten development time and compo-



nent production. The flexible business models of COT, turnkey and partial turnkey, offered by the partnership will enable customers to choose what is right for their ASIC projects", said Carl Das, Director imec ASIC services. ■



Septentrio announces PolaRxS, A State-of-the-Art Ultra Low Noise GNSS Receiver for Ionospheric Scintillation Monitoring



Septentrio announces PolaRxS, an ultra low noise multi-frequency multi-constellation receiver dedicated to ionosphere monitoring and space weather applications.

Powered by Septentrio's next generation multi-frequency receiver engine, PolaRxS offers 136 channels capable of tracking simultaneously GPS, GLONASS, Galileo and SBAS signals in L1, L2, L5 and E5ab/AltBOC bands. Coupled with a state-of-the-art Oven-Controlled Crystal Oscillator (OCXO), the receiver provides an extensive set of specific measurements for ionosphere monitoring, including signal phase and intensity at up to 100 Hz, with a phase noise standard deviation (ϕ_{60}) as low as 0.03 rad.

Proprietary LOCK+ tracking technology guarantees robust tracking of rapid sig-

nal dynamics such as encountered during high scintillation events, while the integrated interference analysis and mitigation module enables installation in difficult radio environments.

As with all Septentrio GNSS receivers, an intuitive Graphical User Interface – RxControl – is provided for data logging and remote control. Specifically for Space Weather and ionosphere monitoring applications, the logging tool is extended for continuous TEC and scintillation indices (ISMR) logging and monitoring.

The advanced user interface coupled with the receiver on-board internet connectivity enable the deployment of monitoring networks at minimal installation and maintenance cost, while its sturdy waterproof housing and low system power consumption (5W) make installation of autonomous stations pos-



sible in the most harsh environment.

"With the currently increasing solar activity heading to a max forecasted in 2013 combined with a reliance to SATCOM and GNSS technologies that have never been so high, ionosphere monitoring and space weather vigilance are becoming of crucial importance" said Peter Grogard, Managing Director of Septentrio. "PolaRxS, which has been developed in close collaboration with prominent members of the ionosphere science community, provides a long awaited, state-of-the-art tool to deploy most effective, low infrastructure-cost, multi-frequency ionosphere and space weather monitoring networks."

Septentrio will start shipping PolaRxSTM in the last quarter of 2010. ■

About Septentrio

Septentrio Satellite Navigation NV designs, manufactures, markets and supports high-end OEM GNSS receivers for demanding professional navigation, positioning and timing applications. Septentrio has an international team of experts in all areas of satellite navigation receiver design and applications.

AnSem strengthens its sales organization in Japan



AnSem, the leading European analog & mixed signal IC design house active in wireless, medical, industrial and communication markets announces the appointment of Kiyohide Ikeda as Japanese Sales Manager.

AnSem is specialized in designing mixed-signal integrated circuits for RF CMOS, high-speed data communication, data

acquisition and ultra low-power & low-voltage applications. It offers custom IC design services as well as full turnkey IC solutions from product idea to the delivery of tested, packaged ASICs.

Ikeda-san will handle Business Development, Marketing & Sales in Japan for semiconductor companies. He brings more than 30 years of Japanese sales and business development experience to AnSem. Having previously worked for LSI Logic, TTP Communications, Motorola

and, more recently, as Sales Manager for Nokia, Ikeda-san has a strong background in large customer account management and a deep knowledge of the Japanese semiconductor market. His experience, his local presence and his strong knowledge of the Japanese high tech market will allow AnSem to better serve its semiconductor customers in Japan.

"The appointment is a next step in managing AnSem's recent growth in Japan and offering a high quality customer account

Wireless sensors in mechatronic applications

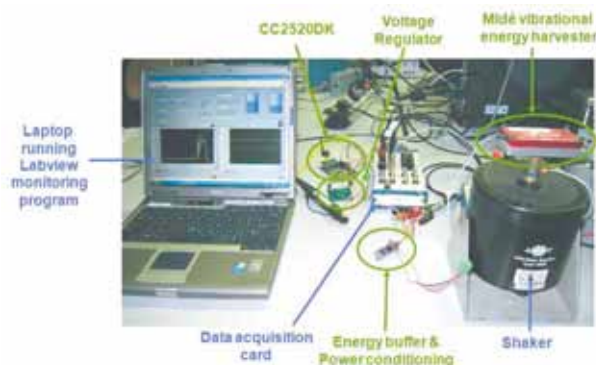


Sensors play an important role in several applications. Machine builders for example apply sensors to provide vital information for the machine control systems to guarantee safe operation. To increase machine functionality, more sensors are required but in many applications although, the extra cost of cabling and installation of these sensors is a blocking factor to initiate these kind of improvement projects. Furthermore, the most interesting places to measure something on a machine are often difficult to reach or they are located on moving parts of the machine (e.g. vibration measurements on a rotating shaft).

Wireless sensors overcome much of the problems associated with wired sensors and therefore have a real breakthrough potential for machine builders. Next to that, if no cables are needed, there is no need for connectors. This means fewer components, less investment cost and less stock keeping items. But even more important, as the installation of cables and connectors is prone to errors, wireless sensors have the potential to increase the machine uptimes significantly. For condition-based and predictive maintenance purposes, wireless sensors can be introduced without stopping the machine as no power shut down is required. Next to that, a network of wireless sensors as part of a troubleshooting kit can be tem-

porarily mounted next to the existing wired sensors to verify their proper functionality. After the intervention, these wireless sensors can be removed easily and be used for a next troubleshooting job.

Although wireless sensors together with mechatronics have been identified as top technologies that will change the world, still a lot of research is needed to get the full benefit of these promising technologies. Recall that wireless technologies for office applications cannot simply be copied for industrial use where robustness and reliable fast response times are of prime importance. The wireless technology for sensors should also be available at low energy consumption in order to enable fully autonomous solutions based on energy harvesting concepts. And of course, wireless sensors should be available at relatively low prices and come in small form factors (often there is very limited space available for integration in the machine). Finally, they should be easy-to-install and -use (plug-and-play), and robust against typical industrial operating environments (vibrations, temperature, oil, dust, EMC, in-band interference, etc.)



The Flanders' Mechatronics Technology Centre (FMTC) has extensive experience in bringing wireless technologies into industrial practice. Knowledge about Bluetooth, Zigbee, WiMedia,..allows us to offer the best fitting technology depending the application and the circumstances. Recently, FMTC demonstrated an energy-autarkic wireless temperature sensor that transmits every 1,25 seconds its measured value while harvesting its energy from the vibrating body on which it is installed. In this way, many potential endangering situations can be avoided and heat losses can be identified in order to operate the machines near optimal energy consumption. As a conclusion, FMTC showed the feasibility to develop wireless temperature sensors and stimulated already many new ideas of wireless sensors for the machine building industry in general. ■

management." said Stefan Gogaert, CEO of AnSem. "The Japanese sales channel strengthens AnSem's position as a leading analog and mixed signal design house in the wireless, medical and industrial markets in Japan and worldwide". ■



About AnSem

AnSem is a fables IC design house founded in 1998. AnSem develops the most advanced customer defined analog and mixed-signal integrated circuits (IC) for RF CMOS wireless applications, high-speed data communication, data acquisition and ultra low-power & low-voltage applications. AnSem also provides turn-key IC solutions including testing and volume IC supply chain management services. AnSem's customers are leading OEM and semiconductor companies active in industrial, medical, wireless & wireline communications and aerospace markets. The design team has completed successfully more than 40 designs the last 12 years. AnSem is ISO9001:2008 certified and is headquartered in Leuven, Belgium.

Sioux achieves 400% productivity gains with Verum ASD:Suite

Verum discontinues own consultancy group in favor of partners



Tools for building mathematically verified software

Sioux (Eindhoven) and Verum Software Technologies BV (Waalre) have closed a commercial partnership agreement around Verum's ASD:Suite software development toolset.

Sioux, the leading innovator in embedded systems and technical automation development services, offers its customers a range of unique business models for outsourced software development. Sioux differentiates itself from many other suppliers through its readiness to bear the risk of an outsourced software development project and its willingness to be paid on a performance related basis. As a result of this powerful combination, Sioux is experiencing a large increase in demand for its services.

In order to meet resultant demand, to enhance its ability to take on complex software development projects and to provide its customers with the highest quality result, Sioux has entered into a partnership agreement with Verum for the use of Verum's ASD:Suite. Ron Willems, Director of Sioux Embedded Systems, said, "We evaluated the ASD:Suite and concluded that it can significantly improve the time to market and productivity of our development projects, whilst also greatly improving the quality of the finished product. By adopting the ASD:Suite we will be able to continue setting the standard for cost and quality effective software development."

Verum is equally pleased with the new partnership. Robert Howe, CEO of Verum, said, "Sioux is on course to changing the way that business is done in the outsourcing market. The systematic use of Verum's ASD:Suite will help them deliver maximum value to their customers."

Sioux's evaluation of the ASD:Suite resulted in more than a 400% improvement in software development productivity. Willems: "We were surprised and

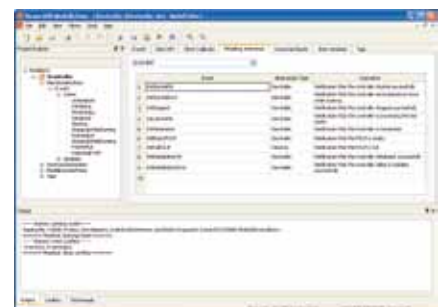
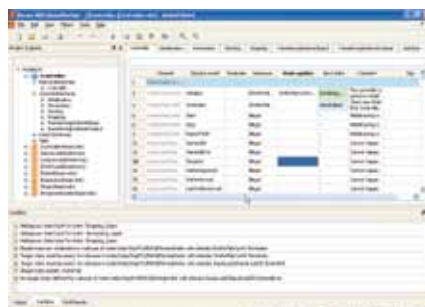
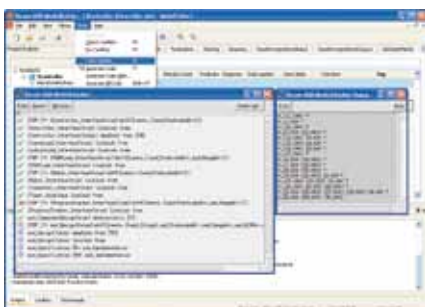
impressed by the results of our evaluation. The business case for ASD is clear." Howe added: "Demand for the ASD:Suite is growing and Verum is increasing its focus on pure product development. We have recently scrapped our consultancy group, creating instead an expanded customer solutions and service team. The demand for ASD related consultancy will therefore shift to our partners and thus we're very pleased to welcome Sioux into the fold." ■

About Verum Software Technologies B.V.

Verum Software Technologies provides a software engineering toolset that enables customers to rapidly develop defect free software for complex systems. Experience has shown that customers using the ASD:Suite can typically reduce the cost of developing their software up to 75% and in equal decrease in time to market, achieving ROI within 3 months. The application of the ASD:Suite also results in a large decrease of the cost-of-non-quality and thereby increased customer satisfaction. The difference between the ASD:Suite and other similar products is that at the heart of ASD's model driven tooling there is a patented formal verification engine that mathematically ensures the completeness and correctness of any software designed and generated using the ASD:Suite.

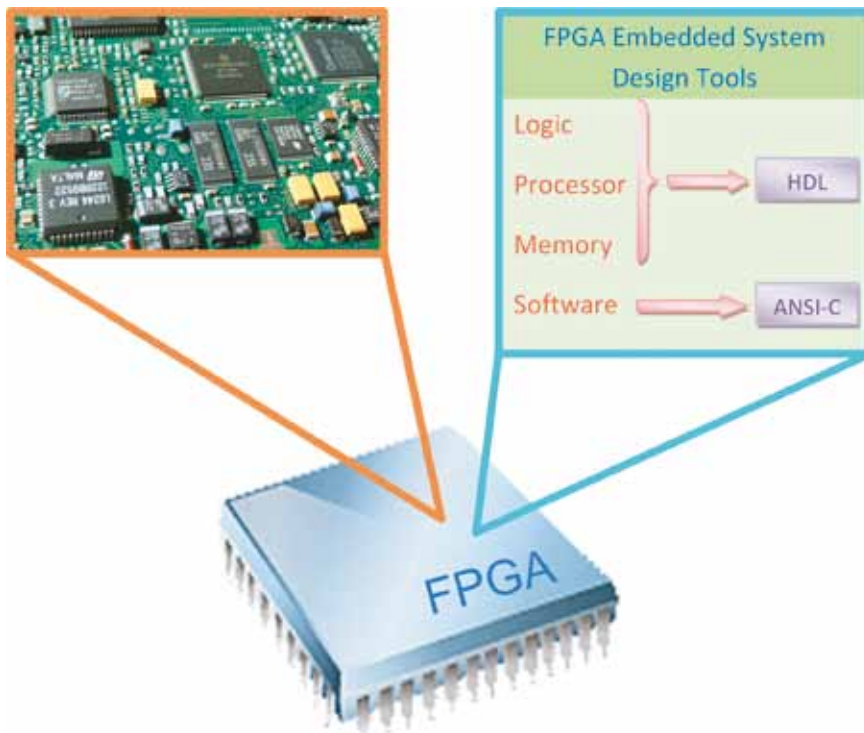
About Sioux Embedded Systems B.V.

Sioux Embedded Systems is member of the Sioux Group. The Sioux Group is a partner in the development of product software and electronics, embedded systems, security and remote solutions for high-tech systems. Innovation, entrepreneurship, professionalism and productivity are central to its approach. Customers notice this in our willingness to co-invest in new developments. Sioux will actively monitor the trends in the world and translates them with creativity and passion for solutions to its customers. Sioux was founded in 1996 and works with over 200 engineers from offices in the Netherlands, Belgium and Russia. The Sioux Group has annual sales of 18 million Euros and annually invests approximately 1 million Euros in knowledge and innovation. 70% of the activities are services (secondment, projects and consultancy) and 30% product development (alliances, licenses and platforms).



An actual example of integrating an embedded system into a high-end FPGA

As the amount of logic cells, building blocks and dedicated components in FPGA's increases, the designs that can be implemented in a single FPGA are becoming larger and more complex. With the use of integrated (on-chip) or synthesized (Intellectual Property) processors, whole embedded systems can be implemented in one chip. This article describes such an application from the field of digital signal processing.



Lab ECOREA (KHBO) is cooperating with Lab NCU (KATHO) within a project on a multichannel ultrasonic real-time analyzer for quality control of materials. The purpose of this research project is to prove the feasibility of a real-time and complete detection of production errors (in plastics, composites, textiles, laminates,...) using state-of-the-art electronic design. In order to validate this research, lab ECOREA is using a high-end FPGA for the implementation of the multichannel ultrasonic analyzer. The implementation requires fast data capturing, processing and high-speed communication to the operator. Additionally, the system consists of multiple sensor pairs each providing data of one part of the material under test. This obliges for parallel data processing,

making an FPGA an excellent development platform for the application.

Each sensor device outputs data at a continuous rate of 120 Mbps. using multiple sensor pairs, total data rates quickly rise above 1 Gbps. Since the sensors aren't placed in the direct environment of the processing FPGA, sensors are combined in groups of four channels and their data is acquired on-site and buffered by low-end FPGA's (one per four channels). These FPGA's subsequently send the buffered data to the processing FPGA using a specifically-developed communication protocol.

Because of the continuous data stream on multiple channels and the real-time processing, the processing is prefer-

ably executed by hardware designed in a Hardware Description Language (HDL). This allows for very precise control of the timing, resulting in much higher processing speeds than can be achieved with a typical embedded processor. Also, for each channel a separate processing pipeline is implemented, so the processing for all channels is performed fully parallel without mutual interference.

The heart of the processing consists of a cross-correlation of the acquired data with a reference pattern. For optimal time utilization, the correlation is performed in the frequency domain implying the use of (inverse) Fast Fourier Transforms. Since there are a lot of multiplications involved with these transforms, dedicated DSP-building blocks (integrated in hardware on the chip) are used. As a result, resources are saved and the operating frequency can highly exceed what is achievable with standard logic cells.

After calculating the necessary parameters of a dataset, the extracted parameters need to be visualized to the operator with, for example, the connection of a display to the FPGA. As an alternative, the FPGA can be connected to a LAN network using a Gigabit Ethernet connection for transfer of the analysis results. The latter provides easy remote access and control of the analyzer, but requires the FPGA to act as a server. Since this requires the FPGA to handle communication protocols like TCP/IP, a soft processor is integrated in the design. This allows the design of a TCP/

continuation from page 13

IP stack in a high-level language like ANSI-C. The communication between the processor and the hardware is actualized by means of high-speed busses. Soft processor, processing hardware and the busses are then merged into a final design and fitted for the FPGA.

As a conclusion, it can be stated that high-end FPGA's are an exceedingly suitable development platform for applications including digital hardware as well as embedded software, such as the example above. The most important advantages are the reduced use of vari-

ous components and the possibility to redesign and reconfigure the embedded system without the necessity to redesign the physical hardware. ■

About ECOREA

ECOREA is a research laboratory of the department of electronics of the University College Bruges-Ostend, Faculty of Engineering Technology. The research domain of the lab ECOREA is the design and implementation of electronic systems, focusing on digital systems with emphasis on the design and evaluation of high-level algorithms, digital signal processing algorithms as well as implementation on FPGA, embedded and DSP-processors.

The research is application-oriented, forming a bridge between fundamental research and application-oriented development, in cooperation with both large companies and SMEs.

Workshop on autonomous, location-aware wireless sensor networks

<http://www.kuleuven.be/lict>



**K.U.Leuven, Dept of Electrical Engineering – ESAT, Leuven, Belgium
October 29, 2010**

LICT kindly invites you to its workshop on "autonomous, location-aware wireless sensor networks" that will take place on Friday, October 29th 2010, at 13:00.

This workshop will be organized on occasion of the end of the SBO project Pinballs: PIN-less BATTERY-Less Low-power microSystems. Besides for presentations by the project partners (K.U.Leuven, AnSem) on the results of the project, there will also be testimonies by industrial speakers (Televic, LMS) about the usage of this kind of technology in their respective application domains.

The complete program will be posted on the LICt website in the near future. Participation to the workshop is free of charge, but advance registration is required.

ABOUT PINBALLS:

PINBALLS: PIN-less BATTERY-Less Low-power microSystems is an SBO-project funded by the IWT, running from 01/04/2006 up to 30/09/2010.

Project partners are: K.U.Leuven - ESAT/MICAS, AnSem NV, Flanders Mechatronics (FMTC) VZW and Vlaams Instituut voor de Logistiek (VIL) VZW.

The overall target of the project was to develop a smart ultra-low-power microsystem platform that is single chip, fully integrated, fully autonomous in its energy provision (battery-less, taking the energy from RF waves in the environment) and connected wirelessly to its environment (pin-less). This device can either be used in identification applications or as a sensor node in a wireless sensor network creating ambient intelligence applications.

Both the autonomously powered tag as well as a battery powered hub were developed in the project by the partners K.U.Leuven and AnSem respectively. Next to the original goal of developing extremely low-power communicating devices, the system has been extended with tag localization capabilities as well, enabling localization with cm precision.

ABOUT LICt:

LICT (Leuven Information and Communication Technology centre) is a cross-departmental center within the K.U.Leuven (Group Science & Technology) that bundles the complementary expertise of electronic engineers, computer scientists, sociologists and law experts from the K.U.Leuven and its association partners that are active in the area of ICT. The mission of the center is to "coordinate and promote top-level research on the design and application of ICT systems, both hardware and software, in support of industry and society". It currently represents about 50 professors and more than 350 researchers from multiple research groups and is organized around seven research lines: "wireless communication systems", "mixed-signal interface systems", "embedded systems and software", "distributed software", "ICT security", "human-machine interaction" and "knowledge technologies".

Conference STW.ICT



Veldhoven, The Netherlands
November 18-19, 2010

The Dutch technology foundation STW organizes the first of an annual STW.ICT conference on Research in Information and Communication Technology on 18-19 November, 2010 at Veldhoven, the Netherlands.

The STW.ICT conference 2010 will encompass the 21st ProRISC workshop on Circuits, Systems and Signal Processing, the 13th SAFE workshop on Semiconductor Advances for Future Electronics and two new workshops: the first PROGRESS workshop on

Embedded Systems & Software and the first Sentinels workshop on Security in ICT. The four workshops will run in parallel in adjacent rooms and with the same program schedule so that it is easy to interchange between the different workshops.

Prof. Dirk Stroobandt of Ghent University (and chairman of the ProRISC workshop): *"The goal of the STW.ICT workshops is to provide the right atmosphere to bring researchers of universities and research institutes closer together with industry and to serve as a platform for discussions between people active in several research domains, from IC-technology and fabrication, over systems and architectures to security and digital signal processing applications and embedded software."*

<http://www.stwplatform.nl/en/stw.ict-conference>

STW.ICT workshops focus on keynote presentations by leaders in the various fields, a few presentations by Ph.D. students that are selected from the submitted abstracts and plenty of time for the poster sessions. In total, about 150 Ph.D. students will present their research through a poster.

Registration

Registration costs between 80 EUR (single day registration) and 275 EUR (two days, including lunches, dinner and hotel room). There are reduced fees for students. Register at <http://www.stwplatform.nl/en/stw.ict-conference> where you will also find more information on the conference STW.ICT and its workshops.

Symposium: A new era for high-level synthesis

<http://flexware.elis.ugent.be/hls-symposium>



Het Pand, Gent, Belgium
December 1, 2010,

In the framework of the FlexWare project (Exploitation of Flexible Hardware Platforms for Massively Parallel Bioinformatics Applications, <http://flexware.elis.ugent.be/>), the FlexWare partners Ghent University, IMEC and Dekimo invite you to the symposium "A new era for high-level synthesis", featuring presentations from renowned speakers on aspects of high-level synthesis automation, design and programming challenges and new computing architectures.

Program

- 13:30 – 14:00: welcome with coffee
- 14:00 – 14:10: introduction by **Dirk Stroobandt** (Ghent University, Belgium): "The FlexWare project in a new era for high-level synthesis"
- 14:10 - 14:50: **Paolo Ienne** (EPFL, Switzerland): "The Irresistible Charm of Automation"
- 14:50 - 15:30: **Jason Villarreal** (Jacquard Computing, Inc., USA): "Design Challenges in the Development of the Riverside Optimizing Compiler for Configurable Computing"
- 15:30 - 16:10: **Paul Stravers** (VectorFabrics, The Netherlands): "Need parallel programs? Think sequential!"
- 16:10 - 16:40: break and posters FlexWare project
- 16:40 - 17:20: **Nigel Topham** (University of Edinburgh, UK): "The Inevitable Complexity of Customization"
- 17:20 - 18:00: **Steve Teig** (Tabula, USA)
- 18:00 - 19:00: closing reception and posters FlexWare project

Registration

The symposium is **free of charge** but registration is mandatory by 21 November. To register, please visit <http://flexware.elis.ugent.be/hls-symposium>. On-site registration will cost 50 EUR administrative fee (to be paid in cash).

How to get there?

The Ghent University congress center Het Pand is easily reached by public transportation. There is also a car park nearby. For those wishing to stay in Ghent, several hotels are available. More information can be found on the website.

Byte Paradigm, new member of DSP Valley • p.1

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Leuven's imec and ICsense partner in European cancer lab-on-chip project • p. 3

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"Nosey Elephant Studios" - Audiovisual laboratory for research and industrial applications • p.4

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Altreonic's scalable and formalized technology gives more for less • p. 4

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http://www.coolflux.com for the CoolFlux DSP core

Enabling GUI Differentiation on Android Devices • p.6

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A Euro-Brazilian consortium to tackle the threat of Ionospheric Scintillation to GNSS operations in Latin America • p.7

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Sigasi announces its University Program • p.7

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Barco presents innovative solution for sub-frame latency processing of single-tile JPEG 2000 images • p.8

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New offices for Irdeto • p.9

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Access to TSMC technologies through leading European partners: imec and DELTA partner to provide comprehensive ASIC solutions • p. 9

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Septentrio announces PolaRxS, A State-of-the-Art Ultra Low Noise GNSS Receiver for Ionospheric Scintillation Monitoring • p.10

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AnSem strengthens its sales organization in Japan • p.10

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Wireless sensors in mechatronic applications • p.11

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Sioux achieves 400% productivity gains with Verum ASD:Suite • p.12

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An actual example of integrating an embedded system into a high-end FPGA • p.13

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